## REMARKS/ARGUMENTS

The Applicants originally submitted Claims 1-16 in the application. In a previous response, the Applicants amended Claims 4, 8 and 12-14. The Examiner has indicated that Claims 8-11 are allowable if rewritten in independent form. In response, the Applicants have amended Claims 7-9 and 14-16. Additionally, the Applicants have added Claims 17-19. Accordingly, Claims 1-19 are currently pending in the application.

### I. Rejection of Claims 1-7 and 12-16 under 35 U.S.C. §102

The Examiner has rejected Claims 1-7 and 12-16 under 35 U.S.C. §102(e) as being anticipated by US Patent No. 6,023,363 to Harada, *et al.* (Harada). The Applicants respectfully disagree. Harada is directed to an optical transmission apparatus and more particularly to a wideband optical receiving apparatus for converting a digital optical signal into an electric signal. (Column 1, lines 4-9). The Examiner cites Figure 6 of Harada to teach each and every element of independent Claims 1 and 7. (Examiner's Final Action, page 2). Figure 6 of Harada, however, does not teach a latch including a clocked trans-admittance stage circuit as recited in Claims 1 and 7. On the contrary, FIGURE 6 of Harada illustrates a feedback amplification circuit that amplifies and converts input voltage signals (non-inverted signal VInT and inverted signal VInB) to current signals at the outputs of the transistor T41, T42. (Column 8, lines 28-33). Instead of receiving a clock signal, the feedback amplification circuit of FIGURE 6 receives the input voltage signals for amplification. FIGURE 6, therefore, does not teach a latch including a clocked trans-admittance stage circuit for receiving a voltage and producing a current output as recited in Claim 1.

Additionally, the office action does not cite any other teachings from Harada that cures the deficiency of FIGURE 6.

Since Harada does not teach each and every element of independent Claims 1 and 7, Harada does not anticipate independent Claim 1 and Claims dependent thereon. Accordingly, the Applicant respectfully requests the Examiner to withdraw the §102 rejection with respect to Claims 1-7 and 12-16 and allow issuance thereof.

Regarding the new claims, Harada also does not teach a latch wherein the clocked trans-admittance stage circuit is further configured to produce a data output as recited in Claim 17. On the contrary, as illustrated in FIGURE 6, a voltage output (OutT, OutB) is provided by the trans-impedance type amplification circuit, not a trans-admittance stage circuit as claimed. (Column 8, lines 40-47 and FIGURE 6).

Additionally, Harada does not teach a latch pair wherein trans-admittance stages of the first and the second combined stages have transistors that lack a common coupling point as recited in Claim 18. Furthermore, Harada does not teach a latch pair wherein transistors of a trans-admittance stage of the first combined stage have collectors directly coupled to the input and the output of the first combined stage. Instead, as illustrated in FIGURE 6, the collectors of T31, T33 and the collectors of T32, T34, are coupled together, respectively. The coupled collectors are then directly connected to Int and InB.

## II. Conclusion

In view of the foregoing amendment and remarks, the Applicants now see all of the Claims currently pending in this application to be in condition for allowance and therefore earnestly solicit a Notice of Allowance for Claims 1-19.

The Applicants request the Examiner to telephone the undersigned attorney of record at (972) 480-8800 if such would further or expedite the prosecution of the present application.

Respectfully submitted,

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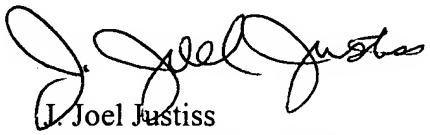

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